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gate-level diagram of the design.Switch level:

This is the lowest level of, logic design

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make a career in digital logic designing then

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career for yourself., Designer must know how data

flows between various registers of the

design.Gate level: The module is

implemented in terms of logic gates and

interconnections between these gates.

Designer should know the gate-level diagram

of the design.Switch level: This is the lowest

level of abstraction. The design is

implemented using switches/transistors.

Designer requires the knowledge of

switch-level implementation details., Here

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that are finance related " and "Set-up and Hold time violation. Frequency divider by 3. NOR gate using CMOS logic. Mod 5 counter. A couple questions about my projects. ". 72% of the interview applicants applied ... , MATHEMATICAL LOGIC EXERCISES Chiara Ghidini and Luciano Serafini Anno Accademico 2013-2014 We thank Annapaola Marconi for her work in previous editions of this booklet., These are some of the favorite static timing analysis and logic design interview questions and they are about making memory elements using the 2:1 MUX. We know the equation of a MUX is :  $Out = S * A + (\bar{S}) * B$ , Digital Logic Design VIVA Questions and Answers :- 1) Explain about setup time and hold time, what will happen if there is setup time and hold time, Most frequently asked VLSI interview questions answered. Also digital design interview questions answered.

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