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results, LVDS CLK CLK Parity Transmitter
LVDS Transmitter, www.ti.com (1) tRSKM is
the timing margin available to allocate to the
transmitter and interconnection skews and
clock jitter. It is defined by $t_c \leq 14 \cdot t_{s,h}$.

ELECTRICAL CHARACTERISTICS,
Low-voltage differential signaling, or LVDS,
also known as TIA/EIA-644, is a technical
standard that specifies electrical
characteristics of a differential, serial
communications protocol., View and
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Interconnects, The JESD204 Interface
Framework is a system-level software and
HDL package targeted at simplifying system
development by providing a performance
optimized IP framework that integrates
complex hardware such as high speed
converters, transceivers and clocks with
various FPGA platforms., Arria V Device
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AV-5V2 2017.12.15 101 Innovation Drive
San Jose, CA 95134, The first seven
receiver signals are entirely analogous to the
transmitter signals, except RX_ER is not
optional and used to indicate the received
signal could not be decoded to valid data.,
Learn about a variety of solutions to
complete the signal chain.,
ComputerWoordenboek. Omdat ik vaak
vragen zoals "Wat is een ..." of "Wat zijn ..."
kreeg, heb ik een woordenboek met
computertaal gemaakt. De onderstaande lijst
bevat al meer dan 4800 termen, afkortingen,
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